IN THE UNITED STATES DISTRICT COURT
FOR THE SOUTHERN DISTRICT OF NEW YORK

INTERNATIONAL BUSINESS MACHINES CORPORATION, **Plaintiff,** **-vs.-** **PLATFORM SOLUTIONS, INC.,** **Defendant.**	**Civil Action No. 06 CV 13565 (CLB)**

JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT

Pursuant to Paragraph 1 of the January 31, 2008 Amended Civil Case Discovery Plan and Scheduling Order, International Business Machines Corporation ("IBM") and Platform Solutions, Incorporated ("PSI") hereby submit the following Joint Claim Construction and Prehearing Statement.

1a. Agreed Constructions

The claim terms, phrases, or clauses for which the parties have agreed on a construction are each listed in attached Exhibit A along with the agreed constructions.

1b. Proposed Constructions for Disputed Terms/Phrases

The parties' respective proposed constructions of each disputed claim term, phrase, or clause, together with an identification of all references from the specification or prosecution history that support that construction, and an identification of any extrinsic evidence on which each intends to rely either to support its proposed construction or to oppose the other party's proposed constructions of the claims (including dictionary definitions, citations to learned treatises, and prior art) are included in the attached Exhibits B and C. The parties have also specified the terms or claim elements that should be governed by 35 U.S.C. § 112(6). The parties have agreed that, in addition to the extrinsic evidence disclosed in Exhibit C, they may each rely on expert declarations on claim construction issues served simultaneously with their briefs. The

parties further reserve the right to supplement the extrinsic record, including information such as deposition testimony of the witnesses, including experts, in this case.

1c. Anticipated Length of Time for the Claim Construction Hearing

The parties anticipate that the hearing will require at least 3 days.

1d. Claim Construction Hearing Witnesses

The parties do not currently agree on whether experts should be called at the Claim Construction hearing. The parties would appreciate the Court's guidance on this issue and on whether, when, and how the Court would like to conduct a technical tutorial (which could be done in person, with or without experts and/or by the submission of interactive computer presentations).

1d. Prehearing Conference

The parties believe that it would be beneficial to discuss the Court's preferences with respect to conducting Claim Construction Hearings, including any preferences concerning technology tutorials and witnesses, at the status conference currently scheduled for April 3, 2008.

Dated: March 28, 2008

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Exhibit A

AGREED CONSTRUCTIONS

U.S. Patent No. 6,654,812

'812 Claim Term	Agreed Construction
generating an IP datagram	In an IP packet, combining a source and destination address with a data payload
network	Communications links between the network ports of two or more computer systems

U.S. Patent No. 5,687,106

'106 Claim Term	Agreed Construction
directly converted	converted without undergoing intermediary conversions
floating point architecture	A way of representing floating point numbers in bits, including the rules for performing mathematical operations on those representations
internal floating point format	The format of a floating point number within a floating point unit (FPU) that is used in the execution of the floating point operations.

U.S. Patent No. 5,825,678

'678 Claim Term	Agreed Construction
condition code	a bit or collection of bits that summarizes the results of the execution of an instruction
floating point data class	One or more categories of floating point numbers possessing one or more specified characteristics

U.S. Patent No. 5,696,709

'709 Claim Term	Agreed Construction
default rounding mode	The rounding mode to be used whenever the current floating point instruction does not specify some other mode
selectively override	selecting from a set of options to override a default operation

Exhibit A

U.S. Patent No. 6,775,789

'789 Claim Term	Agreed Construction
wraps back to zero	resets to zero once the maximum value is exceeded
programmable register	A register whose value can be set by one or more programs
set register instruction	An instruction that sets a given register to a value
considered as one entity	stored contiguously in memory
processor identifier	collection of bits that uniquely specifies a particular processor

U.S. Patent No. 5,987,495

'495 Claim Term	Agreed Construction
a processor is controlled by a program status word	The processor is directed in the execution of a program by the contents of a program status word which indicates the next instruction executed and contains controls constraining the operating state and authority of the program executing under that PSW.
program context	contents of the general registers, the access registers, and the program status word
decoding an instruction	Interpreting the fields of an instruction by a processor
offset	value added to an address to reach the desired address
pointing to a save area	providing the location of an area of main storage in which contents of a program status word and registers are saved

Exhibit A

U.S. Patent No. 5,414,851

'851 Claim Term	**Agreed Construction**
image identifier	a number assigned to each of the plural OSs executing in different resource partitions of the computer system, or the hypervisor
sharing set	a set of control blocks in which each such control block corresponds to the same input/output resource
input/output resource identifier	a collection of bits that identify an I/O resource
hypervisor	a component that supervises the partitions, and programs within such partitions, of the computer electronic complex

U.S. Patent No. 5,953,520

'520 Claim Term	**Agreed Construction**
native	pertaining to the architecture on which the emulator runs
guest	pertaining to the architecture that is being emulated
native addresses	addresses specifying native memory locations
native address space	a range of addresses available to the instructions written for the native architecture
guest address space	a range of addresses available to the instructions written for the guest architecture
native physical addresses	addresses of the native physical memory location
a series of guest instructions	a sequence of one or more guest instructions
emulates	using a data processing system to imitate another data processing system, so that the imitating system accepts the same data, executes the same programs, and achieves the same results as the imitated system.
guest real address	an address that would be used by the emulated data processing system to specify a location in its physical memory, if such a physical memory were available
guest logical address	the number used by a guest program to indirectly reference a location in memory
guest instruction storage	a set of locations in memory containing guest instruction
semantic routine storage	a set of locations in memory containing semantic routines
translating said guest logical address into a guest real address	producing a guest real address to which the given guest logical address corresponds
translating said guest real address into a native physical address	producing a native physical address to which the given guest real address corresponds

Exhibit A

U.S. Patent No. 6,009,261

'261 Claim Term	**Agreed Construction**
emulation	using a data processing system to imitate another data processing system, so that the imitating system accepts the same data, executes the same programs, and achieves the same results as the imitated system.
incompatible	pertaining to the architecture that is being emulated
target	pertaining to the architecture on which the emulator runs
interpreting an instruction	decoding the fields of an instruction by a processor
preprocessing each target instruction	copying or modifying some or all of the target instruction before it is executed

Exhibit B

PROPOSED CONSTRUCTIONS

U.S. Patent No. 6,654,812

'812 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
host-network interface	The communication interface between a host computer and a network.	A hardware component coupled between a host computer and a network port.
saving at said host-network interface	Saving at said host-network interface.	saving on memory located within the host-network interface
(computer) readable program code means embodied therein for causing network communications in a mainframe class data processing system having multiple partitions and a port to a network, the computer readable program code means in the article of manufacture comprising:	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this is a limitation that is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to cause network communications in a mainframe class data processing system having multiple partitions and a port to a network *Structure:* An article of manufacture (*see, e.g.*, 10:46-57 and equivalents thereof) that causes a computer to cause network communications in a mainframe class data processing system having multiple partitions and a port to a network.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing network communications in a mainframe class data processing system having multiple partitions and a port to a network *Structure:* No corresponding structure.

Exhibit B

'812 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
(i) computer readable program code means for causing a computer to effect saving at a host-network interface an internet protocol (IP) address of at least one of the multiple partitions of the mainframe class data processing system	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to effect saving at a host-network interface an internet protocol (IP) address of at least one of the multiple partitions of the mainframe class data processing system *Structure:* An article of manufacture (*see*, *e.g.*, 10:46-57) that causes a computer to effect saving at a host-network interface an internet protocol (IP) address of at least one of the multiple partitions of the mainframe class data processing system (*see*, *e.g.*, Fig. 5, 7:45-8:19), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to effect saving at a host-network interface an internet protocol (IP) address of at least one of the multiple partitions of the mainframe class data processing system *Structure:* No corresponding structure.

Exhibit B

'812 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
(ii) computer readable program code means for causing a computer to effect generating an IP datagram at a first partition of said multiple partitions to be forwarded to a second partition of said multiple partitions using a destination IP address	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to effect generating an IP datagram at a first partition of said multiple partitions to be forwarded to a second partition of said multiple partitions using a destination IP address *Structure:* An article of manufacture (*see*, *e.g.*, 10:46-57) that causes a computer to effect generating an IP datagram at a first partition of said multiple partitions to be forwarded to a second partition of said multiple partitions using a destination IP address (*see*, *e.g.*, step 200 of Fig. 6, 8:33-37; step 300 of Fig. 7, 9:8-10; Fig. 8A, 9:46-57; or Fig. 8B, 10:1-11), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to effect generating an IP datagram at a first partition of said multiple partitions to be forwarded to a second partition of said multiple partitions using a destination IP address *Structure:* No corresponding structure.

Exhibit B

'812 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
(iii) computer readable program code means for causing a computer to effect determining whether said destination IP address for said IP datagram comprises an IP address saved at said host-network interface for said at least one partition, and if so, forwarding the IP datagram directly from said first partition to said second partition of said multiple partitions without employing said network.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to effect determining whether the destination IP address for the IP datagram comprises an IP address saved at the host-network interface for said at least one partition, and if so, forwarding the IP datagram directly from the first partition to the second partition of said multiple partitions without employing the network. *Structure:* An article of manufacture (*see*, *e.g.*, 10:46-57) that causes a computer to effect determining whether the destination IP address for the IP datagram comprises an IP address saved at the host-network interface for said at least one partition, and if so, forwarding the IP datagram directly from the first partition to the second partition of said multiple partitions without employing the network (*see*, *e.g.*, Fig. 5, 8:20-30; or steps 210-240 of Fig. 6, 8:37-48), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to effect determining whether the destination IP address for the IP datagram comprises an IP address saved at the host-network interface for said at least one partition, and if so, forwarding the IP datagram directly from the first partition to the second partition of said multiple partitions without employing the network. *Structure:* No corresponding structure.

Exhibit B

U.S. Patent No. 6,971,002

'002 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
firmware	The term "firmware" is only used as a modifier in the phrase "firmware image" and does not need to be construed separately.	Firmware is "software" stored in a memory chip that holds its content without electrical power, such as, for example, read-only memory (ROM), programmable ROM (PROM), erasable programmable ROM (EPROM), electrically erasable programmable ROM (EEPROM), and non-volatile random access memory (non-volatile RAM).
firmware image	Software copied from non-volatile memory and used to boot a partition.	An instance of a particular firmware.
storing a plurality of different firmware images in said computer system / a plurality of different firmware images being stored in said computer system	Storing more than one distinct firmware image in the computer system.	storing at least two firmware images that are not the same as each other
capable of being executed during a power-on process to boot said computer system	Capable of being executed during the operations performed by a computer system from the time it is turned on until it is ready to run applications to boot said computer system.	able to be executed during the operations performed by a computer system from the time it is turned on until it begins executing the partition firmware

Exhibit B

'002 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
instruction means for storing a plurality of different firmware images in said computer system	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* instructing a computer to store a plurality of different firmware images in the computer system *Structure:* A computer program product stored in a computer recordable-type media (*see*, *e.g.*, 8:4-20) that instructs a computer to store a plurality of different firmware images in the computer system (*see*, *e.g.*, Fig. 3, 6:13-16), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* storing a plurality of different firmware images in said computer system *Structure:* No corresponding structure

Exhibit B

'002 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
instruction means for rebooting one of said plurality of partitions utilizing one of said plurality of firmware images without rebooting other ones of said plurality of partitions	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* instructing a computer to reboot one of the plurality of partitions utilizing one of the plurality of firmware images without rebooting other partitions *Structure:* A computer program product stored in a computer recordable-type media (*see*, *e.g.*, 8:4-20) that instructs a computer to reboot one of the plurality of partitions utilizing one of the plurality of firmware images without rebooting other partitions (*see*, *e.g.*, Fig. 3, 6:58-67; or blocks 422-430 of Fig. 4, 7:30-45), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* rebooting one of said plurality of partitions utilizing one of said plurality of firmware images without rebooting other ones of said plurality of partitions *Structure:* No corresponding structure

Exhibit B

U.S. Patent No. 5,687,106

'106 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
floating point unit	Part of a computer system that performs floating point operations.	That portion of a processor's circuitry that performs floating point calculations
a floating point unit having an internal dataflow	A floating point unit which includes the functions of moving data through the unit and executing floating point operations.	a floating point unit that uses an internal floating point format to perform floating point calculations
supports both said first floating point architecture and said second floating point architecture	Provides the necessary resources for the correct operation of both the first and second floating point architectures.	A floating point unit "supports" a floating point architecture when it can, on its own, perform calculations on floating point numbers of that architecture.
converter	Hardware and/or software that changes data from one format or architecture type to another format or architecture type.	Circuitry within the floating point unit that changes the format or architecture type of a floating point number.

Exhibit B

U.S. Patent No. 5,825,678

'678 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
processor	A portion of a computer system that interprets and executes instructions.	one or more integrated circuits that process coded instructions and perform a task
a floating point processor	A portion of a computer system that interprets and executes floating point instructions.	A processor that contains a floating point unit. A floating point unit is that portion of a processor's circuitry that executes floating point instructions by performing operations on floating point numbers.
a machine instruction	A language construct that specifies an operation and identifies its operands, if any, and can be directly executed by a processor of a computer.	A string of digits that specifies an operation and identifies its operands, if any, and can be directly executed by the processor to which it is directed.
program status word	A defined set of data that indicates the next instruction to be executed and includes the program condition code and program authority, where that data directs the processor in the execution of a program.	The contents of the register that indicates the next instruction to be executed, includes the program condition code and program authority, and directs the processor in the execution of a program.
means for retrieving the floating point number from memory	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* retrieving the floating point number from memory *Structure:* A shared memory computer system (*see*, *e.g.*, Fig. 1, 2:35-38; Fig. 2, 2:39-59) for retrieving the floating point number from memory (*see*, *e.g.*, Fig. 8, 3:63-66), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* retrieving the floating point number from memory *Structure:* No corresponding structure.

Exhibit B

'678 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
means for determining whether the data class of the floating point number is the identified data class by examination of condition of the fields of the floating point number	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* determining whether the data class of the floating point number is the identified data class by examination of condition of the fields of the floating point number *Structure:* A shared memory computer system (*see*, *e.g.*, Fig. 1, 2:35-38; Fig. 2, 2:39-59) for determining whether the data class of the floating point number is the identified data class by examination of condition of the fields of the floating point number (*see*, *e.g.*, Fig. 5, 3:34-45; Fig. 7, 3:49-50; Fig. 8, 3:66-4:5; Fig. 9, 4:9-32), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* determining whether the data class of the floating point number is the identified data class by examination of condition of the fields of the floating point number. *Structure:* Fig. 9, except for the circuitry that connects AND gates to the box marked CC in Fig. 9 (known in the art as a "wired OR gate").
means for setting a condition code in a program status word based upon the determination of whether the data class is the identified data class	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* setting a condition code in a program status word based upon whether the data class is the identified data class *Structure:* A shared memory computer system (*see*, *e.g.*, Fig. 1, 2:35-38; Fig. 2, 2:39-59) for setting a condition code in a program status word based upon whether the data class is the identified data class (*see*, *e.g.*, Fig. 8, 4:5-8; Fig. 9, 4:9-32), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* setting a condition code in a program status word based upon the determination of whether the data class is the identified data class *Structure:* The circuitry that connects the AND gates to the box marked CC in Fig. 9 (known in the art as a "wired OR gate").

Exhibit B

'678 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
An apparatus for determining floating point data class in accordance with claim 1, wherein said means for determining uses a bit mask to determine action to be taken for a particular data class of the floating point number.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* determining whether the data class of the floating point number is the identified data class using a bit mask to determine action to be taken for a particular data class of the floating point number *Structure:* A shared memory computer system (*see*, *e.g.*, Fig. 1, 2:35-38; Fig. 2, 2:39-59) for determining whether the data class of the floating point number is the identified data class using a bit mask to determine action to be taken for a particular data class of the floating point number (*see*, *e.g.*, Fig. 5, 3:34-45; Fig. 7, 3:49-50; Fig. 8, 3:66-4:5; Fig. 9, 4:9-32), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* determining whether the data class of the floating point number is the identified data class by examination of condition of the fields of the floating point number and by using a bit mask to determine action to be taken for a particular data class of the floating point number *Structure:* The bit mask in the upper right hand corner of Fig. 9.

Exhibit B

U.S. Patent No. 5,696,709

'709 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
processor	A portion of a computer system that interprets and executes instructions.	one or more integrated circuits that process coded instructions and perform a task
instruction	A language construct that specifies an operation and identifies its operands, if any.	A string of digits that specifies an operation and identifies its operands, if any, and can be directly executed by the processor to which it is directed.
means for storing a value for specifying one of said floating point rounding modes as a default rounding mode	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* storing a value for specifying one of the floating point rounding modes as a default rounding mode *Structure:* A shared memory computer system (*see*, *e.g.*, Fig. 1, 2:10-13; Fig. 2, 2:13-34) for storing a value for specifying one of the floating point rounding modes as a default rounding mode (*see*, *e.g.*, Fig. 4, 2:54-60), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* storing a value for specifying one of the floating point rounding modes as a default rounding mode *Structure:* Bits 6 and 7 of FPC register 210 in Figure 2.

Exhibit B

'709 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
means for executing a floating point instruction having a field that is operative to selectively override said default rounding mode with another of said rounding modes during execution of said floating point instruction by said processor.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* executing a floating point instruction having a field that is operative to selectively override the default rounding mode with another of said rounding modes during execution of the floating point instruction by the processor. *Structure:* A shared memory computer system (*see*, *e.g.*, Fig. 1, 2:10-13; Fig. 2, 2:13-34) for executing a floating point instruction having a field that is operative to selectively override the default rounding mode with another of said rounding modes during execution of the floating point instruction by the processor (*see*, *e.g.*, Fig. 5, 3:23-4:2; or Fig. 6, 4:11-38), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* executing a floating point instruction having a field that is operative to selectively override said default rounding mode with another of said rounding modes during execution of said floating point instruction by said processor *Structure:* No corresponding structure.

Exhibit B

U.S. Patent No. 6,775,789

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
processor	A portion of a computer system that interprets and executes instructions.	one or more integrated circuits that process coded instructions and perform a task
usable as a current time of day clock value in real-time processing	The sequence value reflects the actual time at which the time value was requested, and is useable as a sequential timestamp where later requests always result in larger values	Representing the actual time of day at which the value can be used by a program
physical clock	Clock implemented in hardware.	A time-of-day (TOD) clock implemented in hardware. A TOD clock embodies the characteristics of uniqueness, monotonicity, and predictable resolution.
instruction	A language construct that specifies an operation and identifies its operands, if any.	A string of digits that specifies an operation and identifies its operands, if any, and can be directly executed by the processor to which it is directed.
register	A part of internal storage having a specified storage capacity and usually intended for a specific purpose.	A hardware storage element in a processor that can be accessed faster than memory.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
means for providing as one part of a sequence value timing information comprising at least one of time-of-day information and date information;	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Providing as one part of a sequence value timing information comprising at least one of time-of-day information and date information. *Structure:* A system (Fig. 1; Col. 5:7-29; Fig. 11; Col. 14:11-24; Fig. 12; Col. 14:25-44; Fig. 13; or Col. 14:35-60) configured to provide as one part of a sequence value timing information comprising at least one of time-of-day information and date information (Fig. 9; Col. 8:62-67; Fig. 10, step 1002; or Col. 9:1-5), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Providing as one part of a sequence value timing information comprising at least one of time-of-day information and date information. *Structure:* Steps 1000-1002 in Fig. 10.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
means for including as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operating system images on one or more processors of said computing environment, wherein said sequence value is usable as a current time of day clock value in real-time processing by one or more processors of the computing environment.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Including as another part of the sequence value selected information usable in making the sequence value unique across a plurality of operating system images on one or more processors of the computing environment *Structure:* A system (Fig. 1; Col. 5:7-29; Fig. 11; Col. 14:11-24; Fig. 12; Col. 14:25-44; Fig. 13; or Col. 14:35-60) configured to include as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operating system images on one or more processors of said computing environment (Fig. 9; Col. 8:62-67; Fig. 10, step 1010; Col. 9:13-15; Col. 11:23-35; or Col. 11:61-12:6), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* including as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operating system images on one or more processors of said computing environment, wherein said sequence value is usable as a current time of day clock value in real-time processing by one or more processors of the computing environment *Structure:* Step 1010 in Fig. 10

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The system of claim 20, further comprising means for providing as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Providing as a further part of the sequence value a placeholder value usable in ensuring that the sequence value is an increasing sequence value, even when a physical clock used to provide the timing information of the sequence value wraps back to zero. *Structure:* A system (Fig. 1; Col. 5:7-29; Fig. 11; Col. 14:11-24; Fig. 12; Col. 14:25-44; Fig. 13; or Col. 14:35-60) configured to provide as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero (Fig. 9; Col. 8:62-67; Fig. 10, step 1000; Col. 9:1-2; or Col. 12:51-64), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* providing as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero *Structure:* Step 1004 in Fig. 10.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The system of claim 20, further comprising means for providing as a further part of said sequence value a processor identifier.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Providing as a further part of the sequence value a processor identifier. *Structure:* A system (Fig. 1; Col. 5:7-29; Fig. 11; Fig. 14:11-24; Fig. 12; Col. 14:25-44; Fig. 13; or Col. 14:35-60) configured to provide as a further part of said sequence value a processor identifier (Fig. 9; Col. 8:62-67; Fig. 10, step 1008; Col. 9:11-15; or Col. 12:7-14), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* providing as a further part of said sequence value a processor identifier *Structure:* Step 1008 in Fig. 10
The system of claim 23, wherein said means for providing comprises means for retrieving, by said instruction, said timing information from a physical clock.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* retrieving, by the instruction, the timing information from a physical clock *Structure:* An instruction used to retrieve said timing information from a physical clock (Fig. 9; Col. 8:62-67; Fig. 10, step 1002; or Col. 9:1-5), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* retrieving, by said instruction, said timing information from a physical clock *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The system of claim 23, ... and wherein said means for including comprises means for retrieving, by said instruction, said selected information from a storage area	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Retrieving, by the instruction, the selected information from a storage area. *Structure:* An instruction used to retrieve said selected information from a storage area (Fig. 9; Col. 8:62-67; Fig. 10, step 1010; Col. 9:13-15; or Col. 8:37-42), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* retrieving, by said instruction, said selected information from a storage area *Structure:* No corresponding structure.
The system of claim 20, further comprising means for receiving said timing information from a physical clock of said computing environment.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Receiving the timing information from a physical clock of the computing environment. *Structure:* A system (Fig. 1; Col. 5:7-29; Fig. 11; Col. 14:11-24; Fig. 12; Col. 14:25-44; Fig. 13; or Col. 14:35-60) configured to receive said timing information from a physical clock of said computing environment (Fig. 9; Col. 8:62-67; Fig. 10, step 1002; or Col. 9:1-5), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* receiving said timing information from a physical clock of said computing environment *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The system of claim 20, further comprising means for obtaining said selected information from a programmable register set by a set register instruction.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Obtaining the selected information from a programmable register set by a set register instruction. *Structure:* A system (Fig. 1 or Col. 5:7-29) configured to obtain said selected information from a programmable register set by a set register instruction (Col. 9:13-15), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* obtaining said selected information from a programmable register set by a set register instruction *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
at least one computer usable medium having computer readable program code means embodied therein for causing the generating of unique sequence values usable within a computing environment, the computer readable program code means in said article of manufacture comprising:	IBM contends this phrase is not governed by 35 U.S.C. § 112, ¶ 6, is not limiting and therefore requires no construction. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function*: causing the generating of unique sequence values usable within a computing environment. *Structure*: An article of manufacture (Col. 14:61-15:4) having computer usable media for causing the generating of unique sequence values usable within a computing environment (Fig. 10 or Col. 8:62-9:15.)	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing the generating of unique sequence values usable within a computing environment *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
computer readable program means for causing a computer to provide as one part of a sequence value timing information comprising at least one of time-of-day information and date information;	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to provide as one part of a sequence value timing information comprising at least one of time-of-day information and date information *Structure:* An article of manufacture (Col. 14:61-15:4) having computer usable media for causing a computer to provide as one part of a sequence value timing information comprising at least one of time-of-day information and date information (Fig. 9; Col. 8:62-67; Fig. 10, step 1002; or Col. 9:1-5), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to provide as one part of a sequence value timing information comprising at least one of time-of-day information and date information *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
computer readable program means for causing a computer to include as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operating system images on one or more processors of said computing environment, wherein said sequence value is usable as a current time of day clock value in real-time processing by one or more processors of the computing environment.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to include as another part of the sequence value selected information usable in making the sequence value unique across a plurality of operating system images on one or more processors of the computing environment *Structure:* An article of manufacture (Col. 14:61-15:4) having computer usable media for causing a computer to include as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operation system images on one or more processors of said computing environment (Fig. 9; Col. 8:62-67; Fig. 10, step 1010; Col. 9:13-15; Col. 11:23-35; or Col. 11:61-12:6), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to include as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operating system images on one or more processors of said computing environment, wherein said sequence value is usable as a current time of day clock value in real-time processing by one or more processors of the computing environment *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The article of manufacture of claim 33, further comprising computer readable program code means for causing a computer to provide as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to provide as a further part of the sequence value a placeholder value usable in ensuring that the sequence value is an increasing sequence value, even when a physical clock used to provide the timing information of the sequence value wraps back to zero *Structure:* An article of manufacture (Col. 14:61-15:4) having computer usable media for causing a computer to provide as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero (Fig. 9; Col. 8:62-67; Fig. 10, step 1000; Col. 9:1-2; or Col. 12:51-64), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to provide as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The article of manufacture of claim 33, further comprising computer readable program code means for causing a computer to provide as a further part of said sequence value a processor identifier.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to provide as a further part of the sequence value a processor identifier. *Structure:* An article of manufacture (Col. 14:61-15:4) having computer usable media for causing a computer to provide as a further part of said sequence value a processor identifier (Fig. 9; Col. 8:62-67; Fig. 10, step 1008; Col. 9:11-15; or Col. 12:7-14), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to provide as a further part of said sequence value a processor identifier *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The article of manufacture of claim 33, wherein said computer readable program code means for causing a computer to provide comprises computer readable program code means for causing a computer to retrieve, by an instruction, said timing information from a physical clock,	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to retrieve, by an instruction, the timing information from a physical clock *Structure:* An article of manufacture (Col. 14:61-15:4) having computer usable media for causing a computer to retrieve, by an instruction, said timing information from a physical clock (Fig. 9; Col. 8:62-67; Fig. 10, step 1002; or Col. 9:1-5), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to retrieve, by an instruction, said timing information from a physical clock *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The article of manufacture of claim 33, ... and wherein said computer readable program code means for causing a computer to include comprises computer readable program code means for causing a computer to retrieve, by said instruction, said selected information from a storage area.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to retrieve, by the instruction, the selected information from a storage area *Structure:* An article of manufacture (Col. 14:61-15:4) having computer usable media for causing a computer to retrieve, by said instruction, said selected information from a storage area (Fig. 9; Col. 8:62-67; Fig. 10, step 1010; Col. 9:13-15; or Col. 8:37-42), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to retrieve, by said instruction, said selected information from a storage area *Structure:* No corresponding structure.

Exhibit B

'789 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
The article of manufacture of claim 33, further comprising computer readable program code means for causing a computer to receive said timing information from a physical clock of said computing environment.	IBM contends this limitation is not governed by 35 U.S.C. § 112, ¶ 6, this limitation needs no construction and should be given its plain and ordinary meaning. If the Court determines this limitation is governed by 35 U.S.C. § 112, ¶ 6, the function and corresponding structure are as follows: *Function:* causing a computer to receive the timing information from a physical clock of the computing environment. *Structure:* An article of manufacture (Col. 14:61-15:4) having computer usable media for causing a computer to receive said timing information from a physical clock of said computing environment (Fig. 9; Col. 8:62-67; Fig. 10, step 1002; or Col. 9:1-5), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* causing a computer to receive said timing information from a physical clock of said computing environment *Structure:* No corresponding structure.

Exhibit B

U.S. Patent No. 5,987,495

'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
processor	A portion of a computer system that interprets and executes instructions.	one or more integrated circuits that process coded instructions and perform a task
instruction	A language construct that specifies an operation and identifies its operands, if any.	A string of digits that specifies an operation and identifies its operands, if any, and can be directly executed by the processor to which it is directed.
program status word	A defined set of data that indicates the next instruction to be executed and includes the program condition code and program authority, where that data directs the processor in the execution of a program.	The contents of the register that indicates the next instruction to be executed, includes the program condition code and program authority, and directs the processor in the execution of a program.
register	A part of internal storage having a specified storage capacity and usually intended for a specific purpose.	A hardware storage element in the processor that can be accessed faster than memory.

Exhibit B

'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means for decoding an instruction from a program executing in said problem state specifying a storage location containing a saved program status word	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Decoding an instruction from a program executing in the problem state specifying a storage location containing a saved program status word *Structure:* Hardware, software , or any suitable combination of the two (Fig. 1; 102 5:4-11; or Col. 7:21-28) configured to decode an instruction from a program executing in said problem state specifying a storage location containing a saved program status word, and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* decoding an instruction from a program executing in said problem state specifying a storage location containing a saved program status word *Structure:* No corresponding structure.

Exhibit B

'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means responsive to said decoding means for restoring from the saved program status word contained at said specified storage location only those fields of the current program status word that are alterable by a program executing in said problem state.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Restoring from the saved program status word contained at the specified storage location only those fields of the current program status word that are alterable by a program executing in the problem state *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102; Col. 7:21-28; Col. 5:4-11) that is configured to restore from the saved program status word contained at said specified storage location only those fields that are alterable by a program executing in said problem state (Figs. 8, step 810; Fig. 6, steps 601-607; Col. 8: 52-58; Col. 9:45-57; or Col. 10:32 – 11:5), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* restoring from the saved program status word contained at said specified storage location only those fields of the current program status word that are alterable by a program executing in said problem state. *Structure:* Steps 606-607 of Fig. 6.

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'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means for determining said storage location using the contents of the register specified by said field.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Determining the storage location using the contents of the register specified by the field. *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102; Col. 5:4-11; or Col. 7:21-28) that is configured to determine the storage location (Fig. 6, step 601; Fig. 2A; Col. 8: 63-65, or Col. 9:15-22), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* determining said storage location using the contents of the register specified by said field. *Structure:* Fig. 2A, 2B.
means for restoring said saved register contents to said register from said save area.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Restoring the saved register contents to the register from the save area. *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102; Col. 7:21-28; or 5:4-11) that is configured to restore the saved register contents to the register in the save area (Fig. 6, steps 602-603; Col. 9:10-12; or Col. 10:46-53), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* restoring said saved register contents to said register from said save area *Structure:* Fig. 6.

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'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means for decoding a program instruction specifying a register selected from said set of registers, said register pointing to a save area containing a saved program status word and saved register contents	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Decoding a program instruction specifying a register selected from the set of registers, the register pointing to a save area containing a saved program status word and saved register contents *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102 5:4-11; or Col. 7:21-28) (*e.g.,* Fig. 1, 102) configured to decode an instruction from a program executing in said problem state specifying a storage location containing a saved program status word, and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* decoding a program instruction specifying a register selected from said set of registers, said register pointing to a save area containing a saved program status word and saved register contents *Structure:* No corresponding structure.
means response to said decoding means for executing said instruction, said executing means comprising:	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Executing the instruction *Structure:* Hardware, software, or any suitable combination configured to execute an instruction (Fig. 1, 102; Col. 5:4-11; Col. 6:66 – 7:77, or Col. 7:21-4), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* executing said instruction *Structure:* No corresponding structure.

Exhibit B

'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means for accessing said save area using the contents of the register specified by said program instruction	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Accessing the save area using the contents of the register specified by the program instruction *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102; Col. 7:21-28; or 5:4-11) that is configured to access the save area using the contents of the register specified by the program instruction (Fig. 2A; Fig. 2B, Fig. 3A; Fig. 6, steps 601, 602, 604, 606; Col. 8: 63-65; Col. 9:5-22; Col. 10:42-45; Col. 10:46-50; Col. 10:54-59; or Col. 10:62-66), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* accessing said save area using the contents of the register specified by said program instruction *Structure:* No corresponding structure.

Exhibit B

'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means for restoring said program status word and said register from the saved program status word and saved register contents contained in said save area to resume execution at the instruction address contained in said saved program status word with the program context defined by said saved program status word and saved register contents.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Restoring the program status word and the register from the saved program status word and saved register contents contained in the save area to resume execution at the instruction address contained in the saved program status word with the program context defined by said saved program status word and saved register contents. *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102; Col. 7:21-28; or 5:4-11) that is configured to restore the program status word and the register from the saved program status word and saved register contents contained in the same area (Fig. 8, step 810; Fig. 6, steps 603, 605, or 607; Col. 9:58-64; Col. 10:50-53; Col. 10:59-61; or Col. 10:66-11:2), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* restoring said program status word and said register from the saved program status word and saved register contents contained in said save area to resume execution at the instruction address contained in said saved program status word with the program context defined by said saved program status word and saved register contents. *Structure:* Fig. 6.

Exhibit B

'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means for adding the specified displacement to the base address contained in said specified register.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Adding the specified displacement to the base address contained in the specified register *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102; Col. 7:21-28; or 5:4-11) configured to add the specified displacement to the base address contained in the specified register (Figs. 3A; 3B; 6, step 601; or Col. 9:38-44; Col. 9:45-57; Col. 10:42-45), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* adding the specified displacement to the base address contained in said specified register *Structure:* No corresponding structure.

Exhibit B

'495 Claim Term	IBM Proposed Construction	PSI's Proposed Construction
means for adding the offset specified by said program instruction to the beginning address of the save area specified by said register.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* Adding the offset specified by the program instruction to the beginning address of the save area specified by the register. *Structure:* Hardware, software, or any suitable combination of the two (Fig. 1; 102; Col. 7:21-28; or 5:4-11) configured to add the offset specified by the program instruction to the beginning address of the save area specified by the register (Figs. 2A, 2B; 3A; 3B; Fig. 6, step 602, 604, or 606; Col. 9:5-15; Col. 10:46-50; Col. 10:54-59; or Col. 10:62-66), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* adding the offset specified by said program instruction to the beginning address of the save area specified by said register *Structure:* No corresponding structure.

Exhibit B

U.S. Patent No. 5,414,851

'851 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
input/output control blocks	Data structures containing information about I/O resources.	a hardware or microprogramming construct which specifies a shared resource to an OS, and may be said to represent an image of the resource to each sharing OS
accessing a control block in said sharing set of input/output control blocks, accessed in the just previous step, with an image identifier of one of said plurality of programs	Using the image identifier to locate the control block.	selecting a control block from a sharing set of input/output control blocks using the image identifier as the selection criterion

Exhibit B

U.S. Patent No. 5,953,520

'520 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
processor	A portion of a computer system that interprets and executes instructions.	one or more integrated circuits that process coded instructions and perform a task
instruction set	The complete set of the operations of the instructions of a computer architecture together with the types of meanings that can be attributed to their operands.	the complete set of the operations of the instructions of a computer together with a description of the types of meanings that can be attributed to their operands
semantic routine	A defined set or sequence of native instructions that, when executed, emulates an associated guest instruction.	a defined sequence of native instructions that, when executed, emulates an associated guest instruction
means, responsive to receipt of said guest memory access instruction for emulation, for translating said guest logical address into a guest real address and for thereafter translating said guest real address into a native physical address	Governed by 35 U.S.C. § 112, ¶ 6 *Function:* translating said guest logical address into a guest real address and for thereafter translating said guest real address into a native physical address *Structure:* A data processing system (Figs. 1, 2, or 3) configured to translate the guest logical address into a guest real address and thereafter to translate the guest real address into a native physical address (Figs. 7 or 8; column and lines: 13:52-14:45; or 14:46-15:7; or 15:56-65), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* translating said guest logical address into a guest real address and for thereafter translating said guest real address into a native physical address *Structure:* Fig. 7, 8, 9

Exhibit B

'520 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
means for executing a semantic routine that emulates said guest memory access instruction utilizing said native physical address.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* executing a semantic routine that emulates said guest memory access instruction utilizing said native physical address *Structure:* A data processing system Figs. 1, 2, or 3) configured to execute a semantic routine that emulates the guest memory access instruction utilizing the native physical address (Fig. 8; column and lines: 11:4-15; 11:26-31; 13:60-14:17; 14:18-20; 15:56-67), and equivalents thereof.	Governed by 35 U.S.C. § 112, ¶ 6. *Function:* executing a semantic routine that emulates said guest memory access instruction utilizing said native physical address *Structure:* Fig. 7, 8, 9

Exhibit B

U.S. Patent No. 6,009,261

'261 Claim Term	IBM's Proposed Construction	PSI's Proposed Construction
patching instruction	An element of a target routine that is used to copy or modify some or all of a target instruction, to enable a guest instruction to be emulated.	an element of a target routine that is used to copy or modify some or all of a target instruction, to enable a guest instruction to be emulated in a dynamic manner each time a guest instruction is encountered
incompatible instruction	A language construct that specifies an operation and identifies its operands, if any, and pertains to the architecture being emulated, which is different than the architecture on which the emulator runs.	A string of digits that specifies an operation and identifies its operands, if any, and would be able to be directly executed by a processor of the emulated data processing system.
target instruction	A language construct that specifies an operation and identifies its operands, if any, and pertains to the architecture on which the emulator runs.	A string of digits that specifies an operation and identifies its operands, if any, and can be directly executed by the processor to which it is directed.
processor	A portion of a computer system that interprets and executes instructions.	one or more integrated circuits that process coded instructions and perform a task
target routine	The set or sequence of target instructions that enable an incompatible instruction to be run on target computer system.	a defined sequence of target instructions performing a function similar to, but not necessarily identically to, a corresponding incompatible instruction

Exhibit C

INTRINSIC AND EXTRINSIC SUPPORT

U.S. Patent No. 6,654,812

'812 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
host-network interface	**Intrinsic Evidence** `812 Patent: Abstract 2:51-3:20 4:4-8 5:6-33 5:44-56 5:61-6:1 6:7-13 Figs. 2-3  `812 Prosecution History: 5/28/03 Response, p. 3 `615 Prosecution History: 8/4/00 Response, pp. 6, 8-13 1/25/01 Response, pp. 10-12 6/20/01 Response, pp. 12, 21 **Extrinsic Evidence** host interface = the interface between a communications network and a host computer (The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, 2000) interface = a shared boundary (The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, 2000)	http://publib.boulder.ibm.com/infocenter/zoslnctr/v1r7/topic/com.ibm.znetwork.doc/znetwork_24.html File history: 5/29/2003 Amendment. U.S. Patent No. 5,740,438. Abstract; Figs. 1-5; 1:1-11:4. International Business Machines Corporation, *8232 LAN Channel Station* (1998). http://www.redbooks.ibm.com/redbooks/GG244252.html International Business Machines Corporation, *TCP/IP Tutorial and Technical Overview* (1992).

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'812 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
	device driver = the software responsible for managing low-level I/O operations for a particular hardware device or set of devices. Contains all the device-specific code necessary to communicate with a device and provides a standard interface to the rest of the system (The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, 2000) host interface = interface between a network and a host computer. *IBM Dictionary of Computing*, 10th Ed., p. 318 © 1994. interface = (1) A shared boundary between two functional units, defined by functional characteristics, signal characteristics, or other characteristics, as appropriate. The concept includes the specification of the connection of two devices having different functions. (2) Hardware, software, or both, that links systems, programs, or devices. *IBM Dictionary of Computing*, 10th Ed., p. 351 © 199 device driver = (1) A file that contains the code needed to use an attached device. (2) A program that enables a computer to communicate with a specific peripheral	

Exhibit C

'812 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
	device; for example, a printer, a videodisc player, or a CD drive. (3) A collection of subroutines that control the interface between I/O device adapters and the processor. *IBM Dictionary of Computing*, 10th Ed., p. 193 © 1994.	
saving at said host network interface	**Intrinsic Evidence** `812 Patent: Abstract 2:51-3:3 4:4-8 5:6-33 5:44-56 5:61-6:1 6:7-13 Figs. 2-3  `812 Prosecution History: 5/28/03 Response, p. 3 `615 Prosecution History: 8/4/00 Response, pp. 6, 8-13 1/25/01 Response, pp. 10-12 6/20/01 Response, pp. 12, 21 **Extrinsic Evidence** host interface = the interface between a communications network and a host computer (The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, 2000)	File history: 5/29/2003 Amendment. U.S. Patent No. 5,740,438. Abstract; Figs. 1-5; 1:1-11:4. International Business Machines Corporation, *8232 LAN Channel Station* (1998). http://www.redbooks.ibm.com/redbooks/GG244252.html International Business Machines Corporation, *TCP/IP Tutorial and Technical Overview* (1992).

Exhibit C

'812 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
	interface = a shared boundary (The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, 2000) host interface = interface between a network and a host computer. *IBM Dictionary of Computing*, 10th Ed., p. 318 © 1994. interface = (1) A shared boundary between two functional units, defined by functional characteristics, signal characteristics, or other characteristics, as appropriate. The concept includes the specification of the connection of two devices having different functions. (2) Hardware, software, or both, that links systems, programs, or devices. *IBM Dictionary of Computing*, 10th Ed., p. 351 © 1994.	
(computer) readable program code means embodied therein for causing network communications in a mainframe class data processing system having multiple partitions and a port to a network, the computer readable program code means in the article of manufacture comprising:	**Intrinsic Evidence** `812 Patent: 10:46-57 12:27-34	

Exhibit C

'812 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
(i) computer readable program code means for causing a computer to effect saving at a host-network interface an internet protocol (IP) address of at least one of the multiple partitions of the mainframe class data processing system	**Intrinsic Evidence** `812 Patent: 7:45-8:19 10:46-57 Fig. 5  `812 Prosecution History: 5/28/03 Response, p. 3	
(ii) computer readable program code means for causing a computer to effect generating an IP datagram at a first partition of said multiple partitions to be forwarded to a second partition of said multiple partitions using a destination IP address	**Intrinsic Evidence** `812 Patent: 8:33-37 9:8-10 9:46-57 10:1-11 10:46-57 Figs. 6, 7, 8A, 8B  `812 Prosecution History: 5/28/03 Response, p. 5	
(iii) computer readable program code means for causing a computer to effect determining whether said destination IP address for said IP datagram comprises an IP address saved at said host-network interface for said at least one partition, and if so, forwarding the IP datagram directly from said first partition to said second partition of said multiple partitions without employing said network.	**Intrinsic Evidence** `812 Patent: 7:45-8:7 8:20-48 9:41-45 10:46-57 Figs. 3, 5, 6  `812 Prosecution History: 5/28/03 Response, pp. 2-5	

Exhibit C

U.S. Patent No. 6,971,002

'002 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**

Exhibit C

'002 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
firmware	**Intrinsic Evidence** `002 Patent: 1:59-65 2:57-3:11 5:62-6:3 6:11-33 6:42-47 6:53-8:20 Figs. 3-5  `002 Prosecution History: 10/15/2004 Response to OA, pp. 9-10 5/17/2005 Appeal Brief, pp. 10-13 **Extrinsic Evidence** firmware = broadly, the system software stored in a computer's read-only memory (ROM) or elsewhere in the computer's circuitry, such as the BIOS chip in IBM PC-compatible computers (Webster's New World Dictionary of Computer Terms, Eighth Edition, 2000)	6:22-28 U.S. Patent No. 6,725,317 U.S. Patent No. 6,973,517 U.S. Patent No. 6,834,340 Compact Oxford English Dictionary, "Firmware" ("permanent software programmed into a read-only memory"), *at* http://www.askoxford.com/concise_oed/firmware IBM's Preliminary Comments on PSI's complaint in Case no COMP/C-3/3951/Platform Solutions, Inc/IBM before the European Commission Competition Directorate-General at 2. IBM Technical Disclosure Bulletin, vol. 36, No. 03, Mar. 1993, "Sharing Read-Only Memory among Multiple Logical Partitions", pp. 303-304. IBM Technical Disclosure Bulletin, vol. 39, No. 12, Dec. 1996, "Highly Parallel Coupling Facility Emulator/Router with Shadowed Link Buffers", 2 pages. IBM Technical Disclosure Bulletin, vol. 39, No. 06, Jun. 1996, "Coordinating Multiple Server Partitions to Enter Power-Save State", pp. 235-239.

Exhibit C

'002 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
firmware image	**Intrinsic Evidence** `002 Patent: 1:30-42 1:59-65 2:57-3:11 5:62-6:3 6:11-33 6:42-47 6:53-8:20 Figs. 3-5  `002 Prosecution History: 10/15/2004 Response to OA, pp. 9-10 5/17/2005 Appeal Brief, pp. 10-13 **Extrinsic Evidence** firmware = broadly, the system software stored in a computer's read-only memory (ROM) or elsewhere in the computer's circuitry, such as the BIOS chip in IBM PC-compatible computers (Webster's New World Dictionary of Computer Terms, Eighth Edition, 2000)	1:60-61; 2:11-13; 6:11-16; 6:22-28; IBM Technical Disclosure Bulletin, vol. 36, No. 03, Mar. 1993, "Sharing Read-Only Memory among Multiple Logical Partitions", pp. 303-304. IBM Technical Disclosure Bulletin, vol. 39, No. 12, Dec. 1996, "Highly Parallel Coupling Facility Emulator/Router with Shadowed Link Buffers", 2 pages. IBM Technical Disclosure Bulletin, vol. 39, No. 06, Jun. 1996, "Coordinating Multiple Server Partitions to Enter Power-Save State", pp. 235-239.

Exhibit C

'002 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
storing a plurality of different firmware images in said computer system / a plurality of different firmware images being stored in said computer system	**Intrinsic Evidence** `002 Patent: 1:59-2:13 2:57-63 5:62-6:47 7:1-8:3 Figs. 3-5  `002 Prosecution History: 10/15/2004 Response to OA, pp. 9-10 5/17/2005 Appeal Brief, pp. 10-13	Abstract; Fig. 4; Fig. 5; 1:10-16; 1:66-2:64; 3:1-3; 6:42-48; 7:1-8:30.
capable of being executed during a power-on process to boot said computer system	**Intrinsic Evidence** `002 Patent: 3:1-8 5:15-27 6:58-7:45 Figs. 2, 4  `002 Prosecution History: 10/15/2004 Response to OA, pp. 9-10 5/17/2005 Appeal Brief, pp. 11-12	Fig. 4; Fig. 5; 1:59-65; 2:38-48; 3:4-11; 5:44-54; 6:34-47; 7:45-58.

Exhibit C

'002 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
instruction means for storing a plurality of different firmware images in said computer system	**Intrinsic Evidence** `002 Patent: 1:59-2:13 2:57-63 3:12-6:47 7:1-8:20 Figs. 1-5  `002 Prosecution History: 10/15/2004 Response to OA, pp. 9-10 5/17/2005 Appeal Brief, pp. 10-13	
instruction means for rebooting one of said plurality of partitions utilizing one of said plurality of firmware images without rebooting other ones of said plurality of partitions	**Intrinsic Evidence** `002 Patent: 1:59-2:13 2:57-3:11 3:12-6:47 6:58-8:20 Figs. 1-5  `002 Prosecution History: 10/15/2004 Response to OA, pp. 9-10 5/17/2005 Appeal Brief, pp. 11-12	

Exhibit C

U.S. Patent No. 5,687,106

'106 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
floating point unit	**Intrinsic Evidence** `106 Patent: 3:53-15:63 20:47-56 Figs. 1-4	Phillip A. Laplante, "Comprehensive Dictionary of Electrical Engineering" (CRC Press 2005): "floating-point unit. a circuit that performs floating-point computations, which is generally addition, subtraction, multiplication, or division." "Microsoft Press Computer Dictionary" (Microsoft Press 1997): "A circuit that performs floating-point calculations." http://www-306.ibm.com/software/globalization/terminology/tu.jsp#x2042528 (Unit: "A mechanical, electrical, or electronic piece of equipment for a special purpose.") Abstract; Fig. 1-5; 2:8-29; 3:53-20:56.

Exhibit C

'106 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
a floating point unit having an internal dataflow	**Intrinsic Evidence** `106 Patent: ABSTRACT 1:57-65 2:2-5 3:18-45 3:53-5:39 15:37-63 20:47-56 Fig. 1 **Extrinsic Evidence** **Data Flow** - The movement of data through a system from its entry to its destination. *Microsoft Press Computer Dictionary*, 2nd Ed., p. 107 © 1994.	Abstract; Fig. 1; 1:56-2:29; 3:17-20:56.

Exhibit C

'106 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
supports both said first floating point architecture and said second floating point architecture	**Intrinsic Evidence** `106 Patent: 1:6-8 1:22-45 1:58-63 2:32-36 3:20-31 4:60-62 20:39-43 20:47-56 **Extrinsic Evidence** **Support** - In system development, to provide the necessary resources for the correct operation of a functional unit. *IBM Dictionary of Computing*, 10th Ed., p. 663 © 1994.	Abstract; Fig. 1; 1:56-2:29; 3:17-20:56. *Alpha Architecture Reference Manual*, Richard L. Sites, ed., Digital Press, 1992. ISBN 1-55558-098-X. U.S. Patent 5,161,117. U.S. Patent 4,949,291.

Exhibit C

'106 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
converter	**Intrinsic Evidence** `106 Patent: 3:46-15:63 20:47-56 Figs. 1-4  `106 Prosecution History: 12/11/96 Amendment, p. 13 U.S. Pat. No. 5,757,682 (incorporated by reference) at 11:50-17:21, Figs. 8-9 **Extrinsic Evidence** **Converter** - A device that can convert impulses from one form to another, such as analog to digital, parallel to serial, one code to another, or one protocol to another. See code converter, data converter. *IBM Dictionary of Computing*, 10th Ed., p. 149 © 1994. **Data converter** - A functional unit that transforms data from one representation to an equivalent representation. *IBM Dictionary of Computing*, 10th Ed., p. 168 © 1994.	2:14-15; Fig. 1; 3:19-5:39; 5:40-20:38. U.S. Patent 5,161,117. U.S. Patent 4,949,291.

Exhibit C

U.S. Patent No. 5,825,678

'678 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
processor	**Intrinsic Evidence** `678 Patent: 2:39-59 Fig. 2 **Extrinsic Evidence** **Processor** - (1) In a computer, a functional unit that interprets and executes instructions. A processor consists of at least an instruction control unit and an arithmetic and logic unit. *IBM Dictionary of Computing*, 10th Ed., p. 533 © 1994.	IBM Dictionary of Computing, "processor." Oxford English Dictionary, "processor," "central." October 1, 1989 license agreement between IBM and Intel The document bearing Bates number IBMPSI10152467 http://www.research.ibm.com/journal/rd/511/berger.html http://www-03.ibm.com/systems/browse/inpro/ http://www-03.ibm.com/systems/browse/power/index.html http://www-03.ibm.com/systems/browse/amdpro/index.html?cm_re=masthead-_-products-_-sys-amd https://www-304.ibm.com/systems/support/supportsite.wss/docdisplay?lndocid=MIGR-39433&brandind=5000008

Exhibit C

'678 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
		http://www-304.ibm.com/jct09002c/isv/tech/faq/individual?oid=2:85007 http://www-03.ibm.com/press/us/en/pressrelease/21580.wss http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ119954 http://www.intel.com/pressroom/kits/itanium2/ Fig. 1-2; 2:13-17; 2:34-36; 3:52-53; 4:63-65.
a floating point processor	**Intrinsic Evidence** `678 Patent: 2:39-59 Fig. 2 **Extrinsic Evidence** **Processor** - (1) In a computer, a functional unit that interprets and executes instructions. A processor consists of at least an instruction control unit and an arithmetic and logic unit. *IBM Dictionary of Computing*, 10th Ed., p. 533 © 1994.	IBM Dictionary of Computing, "processor." Oxford English Dictionary, "processor," "central." October 1, 1989 license agreement between IBM and Intel The document bearing Bates number IBMPSI10152467 http://www.research.ibm.com/journal/rd/511/berger.html

Exhibit C

'678 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
		http://www-03.ibm.com/systems/browse/inpro/ http://www-03.ibm.com/systems/browse/power/index.html http://www-03.ibm.com/systems/browse/amdpro/index.html?cm_re=masthead-_-products-_-sys-amd https://www-304.ibm.com/systems/support/supportsite.wss/docdisplay?lndocid=MIGR-39433&brandind=5000008 http://www-304.ibm.com/jct09002c/isv/tech/faq/individual?oid=2:85007 http://www-03.ibm.com/press/us/en/pressrelease/21580.wss http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ119954 http://www.intel.com/pressroom/kits/itanium2/

Exhibit C

'678 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
		Phillip A. Laplante, "Comprehensive Dictionary of Electrical Engineering" (CRC Press 2005): "floating-point unit. a circuit that performs floating-point computations, which is generally addition, subtraction, multiplication, or division." "Microsoft Press Computer Dictionary" (Microsoft Press 1997): "A circuit that performs floating-point calculations." http://www-306.ibm.com/software/globalization/terminology/tu.jsp#x2042528 (Unit: "A mechanical, electrical, or electronic piece of equipment for a special purpose.") Fig. 1; 2:34-36; 3:52-53; 4:63-65

Exhibit C

'678 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
a machine instruction	**Intrinsic Evidence** `678 Patent: ABSTRACT 1:59-67 3:19-45 Fig. 5 U.S. Pat. No. 5,687,106 (incorporated by reference) at 3:57-4:1 **Extrinsic Evidence** **Instruction** - in digital computer operations, a set of bits defining an operation. Consists of an operation code specifying the operation to be performed, one or more operands or their address, and one or more modifiers or their addresses (to modify the operand or its address). *The Illustrated Dictionary of Electronics*, 7th Ed., p. 363, © 1997. **Instruction** - (1) A language construct that specifies an operation and identifies its operands, if any. *IBM Dictionary of Computing*, 10th Ed., p. 346 © 1994. **Machine Instruction** - (1) An instruction that can be directly executed by a processor of a computer. A machine instruction is an element of a machine language. *IBM Dictionary of Computing*, 10th Ed., p. 408 © 1994.	IBM Dictionary of Computing, "computer instruction," "computer instruction set," "instruction," "machine instruction." *Encyclopedia of Computer Science* (3d ed.) at 684. http://www-306.ibm.com/software/globalization/terminology/ij.jsp The document bearing Bates number IBMPSI03906987 The document bearing Bates number IBMPSI10152467 Abstract; 1:41-67; 2:21-23; 2:38-59; 3:9-11; 3:19-33; 3:50-60.

Exhibit C

'678 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
program status word	**Intrinsic Evidence** `678 Patent: 2:39-3:11 4:33-36 Figs. 2 and 3 Enterprise Systems Architecture/390 Principles of Operation (1994), Order No. SA22-7201-02, Chapter 4 **Extrinsic Evidence** **Program Status Word (PSW)** - An area in storage used to indicate the order in which instructions are executed, and to hold and indicate the status of a computer system. Synonymous with processor status word. *IBM Dictionary of Computing*, 10th Ed., p. 539, © 1994. **Program Status Word (PSW)** - (A) A computer word that contains information specifying the current status of a computer program. The information may include error indicators, the address of the next instruction to be executed, currently enabled interrupts, and so on. *The IEEE Standard Dictionary of Electrical and Electronics Terms*, 6th Ed., p. 827, IEEE Std 100-1996. T3 Technologies Liberty Series ML 5.1 Operator Station User Guide	http://www-306.ibm.com/software/globalization/terminology/op.jsp#p15 IBM Dictionary of Computing, "program status word." z/Architecture Principles of Operation at 2-2 through 2-5. Fig. 1; Fig. 2; Fig. 3; 1:43-47; 2:13-3:12.

Exhibit C

'678 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
means for retrieving the floating point number from memory	**Intrinsic Evidence** `678 Patent: 2:35-59 3:19-46 3:63-66 Figs. 1, 2, 5, 7	
means for determining whether the data class of the floating point number is the identified data class by examination of condition of the fields of the floating point number	**Intrinsic Evidence** `678 Patent: 1:54-2:6 2:35-59 3:19-46 3:49-4:32 Figs. 1, 2, 5, 7-9	*Linking Language:* 2:31-32.
means for setting a condition code in a program status word based upon the determination of whether the data class is the identified data class	**Intrinsic Evidence** `678 Patent: 1:54-2:6 2:35-59 3:19-46 3:52-4:32 Figs. 1, 2, 5, 7-9	*Linking Language:* 2:31-32.
An apparatus for determining floating point data class in accordance with claim 1, wherein said means for determining uses a bit mask to determine action to be taken for a particular data class of the floating point number.	**Intrinsic Evidence** `678 Patent: 1:54-2:6 2:35-59 3:19-46 3:49-4:32 Figs. 1, 2, 5, 7-9	*Linking Language:* 2:31-32.

Exhibit C

U.S. Patent No. 5,696,709

'709 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
processor	**Intrinsic Evidence** `709 Patent: 2:10-34 2:41-52 3:23-43 4:4-38 Figs. 1, 2, 4, 5, 6  `709 Prosecution History: 9/13/96 Amendment, pp. 4-7 **Extrinsic Evidence** **Processor** - (1) In a computer, a functional unit that interprets and executes instructions. A processor consists of at least an instruction control unit and an arithmetic and logic unit. *IBM Dictionary of Computing*, 10th Ed., p. 533 © 1994.	IBM Dictionary of Computing, "processor." Oxford English Dictionary, "processor," "central." October 1, 1989 license agreement between IBM and Intel The document bearing Bates number IBMPSI10152467 http://www.research.ibm.com/journal/rd/511/berger.html http://www.research.ibm.com/journal/rd/511/berger.html http://www-03.ibm.com/systems/browse/inpro/ http://www-03.ibm.com/systems/browse/power/index.html http://www-03.ibm.com/systems/browse/amdpro/index.html?cm_re=masthead-_-products-_-sys-amd https://www-304.ibm.com/systems/support/supportsite.wss/docdisplay?lndocid=MIGR-

Exhibit C

'709 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
		39433&brandind=5000008 http://www-304.ibm.com/jct09002c/isv/tech/faq/individual?oid=2:85007 http://www-03.ibm.com/press/us/en/pressrelease/21580.wss http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ119954 http://www.intel.com/pressroom/kits/itanium2/ Fig. 1; Fig. 2; 2:10-49.

Exhibit C

'709 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
instruction	**Intrinsic Evidence** `709 Patent: ABSTRACT 1:42-46 2:10-26 3:23-4:38 Figs. 5, 6  `709 Prosecution History: 9/24/96 Response to OA at 4-5 **Extrinsic Evidence** **Instruction** - in digital computer operations, a set of bits defining an operation. Consists of an operation code specifying the operation to be performed, one or more operands or their address, and one or more modifiers or their addresses (to modify the operand or its address). *The Illustrated Dictionary of Electronics*, 7th Ed., p. 363, © 1997. **Instruction** - (1) A language construct that specifies an operation and identifies its operands, if any. *IBM Dictionary of Computing*, 10th Ed., p. 346 © 1994.	IBM Dictionary of Computing, "computer instruction," "computer instruction set," "instruction," "machine instruction." *Encyclopedia of Computer Science* (3d ed.) at 684. http://www-306.ibm.com/software/globalization/terminology/ij.jsp The document bearing Bates number IBMPSI03906987 The document bearing Bates number IBMPSI10152467 Abstract; Fig. 5; 1:39-47; 2:10-34; 2:61-4:48; 4:62-64.
means for storing a value for specifying one of said floating point rounding modes as a default rounding mode	**Intrinsic Evidence** `709 Patent: 1:39-46 2:26-34 2:54-57 Figs. 2, 4	*Linking Language:* Fig. 4; 1:57-67.

Exhibit C

'709 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
means for executing a floating point instruction...	**Intrinsic Evidence** `709 Patent: 1:39-46 2:13-34 3:22-4:39 Figs. 2, 5, 6	

Exhibit C

U.S. Patent No. 6,775,789

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
processor	**Intrinsic Evidence** `789 Patent: 5:4-28 5:41-6:9 6:11-31 7:56-65 14:19-60 Figs. 1, 3, 11, 12, 13 **Extrinsic Evidence** **Processor** - (1) In a computer, a functional unit that interprets and executes instructions. A processor consists of at least an instruction control unit and an arithmetic and logic unit. *IBM Dictionary of Computing*, 10th Ed., p. 533 © 1994.	IBM Dictionary of Computing, "processor." Oxford English Dictionary, "processor," "central." October 1, 1989 license agreement between IBM and Intel The document bearing Bates number IBMPSI10152467 http://www.research.ibm.com/journal/rd/511/berger.html http://www-03.ibm.com/systems/browse/inpro/ http://www-03.ibm.com/systems/browse/power/index.html http://www-03.ibm.com/systems/browse/amdpro/index.html?cm_re=masthead-_-products-_-sys-amd https://www-304.ibm.com/systems/support/supportsite.

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
		wss/docdisplay?lndocid=MIGR-39433&brandind=5000008 http://www-304.ibm.com/jct09002c/isv/tech/faq/individual?oid=2:85007 http://www-03.ibm.com/press/us/en/pressrelease/21580.wss http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ119954 http://www.intel.com/pressroom/kits/itanium2/ Fig. 1; Fig. 2; Fig. 3; 2:21-4:38; 7:56-8:37; 13:5-14:60.
usable as a current time of day clock value in real-time processing	**Intrinsic Evidence** `789 Patent: 1:28-2:10 6:31-7:3 12:36-64  `789 Prosecution History: 7/1/02 Response, pp. 15-20 2/10/03 Preliminary Amendment, pp. 11-14	File history: 3/1/2004 Response. IBM Dictionary of Computing, "real-time processing," "time-of-day clock." http://www-306.ibm.com/software/globalization/terminology/qr.jsp#r17 Jochen Liedtke et al., *OS-Controlled Cache*

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
	7/14/03 Response, pp. 2-4 1/6/04 Response, pp. 10-13 3/3/04 Preliminary Amendment, pp. 10-12	*Predictability for Real-Time Systems*, Proceedings of the 3rd IEEE Real-Time Technology and Applications Symposium 213 (1997). Ajay D. Kshemkalyani, *Synchronization for Distributed Real-time Applications*, Proceedings of the 1997 Joint Workshop on Parallel and Distributed Real-Time Systems 81 (1997). Anant Jhingran, *Why commercial database systems are not real-time systems*, Proceedings of the workshop on Databases: active and real-time 50 (1996). IBM Tech. Disc. Bul. v23n8 pgs. 3819-3820 U.S. Patent No. 3,999,169. U.S. Patent No. 5,416,921. 1:27-41.
physical clock	**Intrinsic Evidence** `789 Patent: 4:66-5:3 6:37-44 6:66-7:8	1:58-67; 6:37-40; 9:2-5.

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
instruction	**Intrinsic Evidence** `789 Patent: 8:22-30 8:43-9:43 11:5-60 Figs. 7, 8, 9, 10 **Extrinsic Evidence** **Instruction** - in digital computer operations, a set of bits defining an operation. Consists of an operation code specifying the operation to be performed, one or more operands or their address, and one or more modifiers or their addresses (to modify the operand or its address). *The Illustrated Dictionary of Electronics*, 7th Ed., p. 363, © 1997. **Instruction** - (1) A language construct that specifies an operation and identifies its operands, if any. *IBM Dictionary of Computing*, 10th Ed., p. 346 © 1994.	IBM Dictionary of Computing, "computer instruction," "computer instruction set," "instruction," "machine instruction." *Encyclopedia of Computer Science* (3d ed.) at 684. http://www-306.ibm.com/software/globalization/terminology/ij.jsp The document bearing Bates number IBMPSI03906987 The document bearing Bates number IBMPSI10152467 1:42-14:9.

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
register	**Intrinsic Evidence** `789 Patent: 6:37-44 8:6-53 9:14-16 13:54-14:4 Figs. 6, 8, 10 **Extrinsic Evidence** **register** - A part of internal storage having a specified storage capacity and usually intended for a specific purpose. *IBM Dictionary of Computing*, George McDaniel, Tenth Edition (August 1993), (c) 1994, ISBN 0-07-031489-6, p. 539.	Encyclopedia of Computer Science, "register." Oxford English Dictionary, "register." The Academic Press Dictionary of Science and Technology, "register." American Heritage Dictionary of the English Language, "register" ("A part of the central processing unit used as a storage location."), *at* http://www.bartleby.com/61/55/R0125500.html. Free On-Line Dictionary of Computing, "register", *at* http://foldoc.org/?register. Fig. 6; Fig. 10; 4:44-59.

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
means for providing as one part of a sequence value timing information comprising at least one of time-of-day information and date information;	**Intrinsic Evidence** `789 Patent: 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:4-12 7:13-55 8:43-53 8:62-67 9:1-5 14:9-60 14:61-15:17 Figs. 1, 4, 5, 8, 9, 10, 11, 12, 13	*Linking Language:* 4:57-59.
means for including as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operating system images on one or more processors of said computing environment, wherein said sequence value is usable as a current time of day clock value in real-time processing by one or more processors of the computing environment.	**Intrinsic Evidence** `789 Patent: 5:7- 29 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:66-8:5 8:6-12 8:13-21 8:43-53 8:62-67 9:13-15 11:23-35 11:61-12:6 14:9-60 Figs. 1, 4, 6, 7, 8, 9, 10, 11, 12, 13	*Linking Language:* 4:57-59.
The system of claim 20, further comprising	**Intrinsic Evidence**	*Linking Language:* 4:57-59.

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
means for providing as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero.	`789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 6:31-7:3 8:43-53 8:62-67 9:1-2 12:42-50 12:51-64 14:9-60 Figs. 1, 4, 8, 9, 10, 11, 12, 13	
The system of claim 20, further comprising means for providing as a further part of said sequence value a processor identifier.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 7:56-65 8:43-53 8:62-67 9:11-15 12:7-14 12:15-26 14:9-60 Figs. 1, 4, 8, 9, 10, 11, 12, 13	*Linking Language:* 4:57-59.

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
The system of claim 23, wherein said means for providing comprises means for retrieving, by said instruction, said timing information from a physical clock.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:4-12 7:13-55 8:43-53 8:62-67 9:1-5 Figs. 1, 4, 5, 8, 9, 10, 11, 12, 13	
The system of claim 23, ... and wherein said means for including comprises means for retrieving, by said instruction, said selected information from a storage area	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:66-8:5 8:6-12 8:13-21 8:22-29 8:37-42 8:43-53 8:62-67 9:13-15 Figs. 1, 4, 5, 8, 9, 10, 11, 12, 13	
The system of claim 20, further comprising means for receiving said timing information from a physical clock of said computing environment.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60	

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
	6:16-30 7:4-12 7:13-55 8:43-53 8:62-67 9:1-5 14:9-60 Figs. 1, 4, 5, 8, 11, 12, 13	
The system of claim 20, further comprising means for obtaining said selected information from a programmable register set by a set register instruction.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 8:6-30 9:13-15 9:16-11:60 Figs. 1, 5, 6, 7, 9, 11, 12, 13	
at least one computer usable medium having computer readable program code means embodied therein for causing the generating of unique sequence values usable within a computing environment, the computer readable program code means in said article of manufacture comprising:	**Intrinsic Evidence** `789 Patent: Abstract 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 4:57-59 6:16-8:61 8:62-9:15 14:61-15:4 Figs. 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
computer readable program means for causing a computer to provide as one part of a sequence value timing information comprising at least one of time-of-day information and date information;	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:4-12 7:13-55 8:43-53 8:62-67 9:1-5 14:61-15:4 Figs. 1, 4, 5, 8, 9, 10, 11, 12, 13	
computer readable program means for causing a computer to include as another part of said sequence value selected information usable in making said sequence value unique across a plurality of operating system images on one or more processors of said computing environment, wherein said sequence value is usable as a current time of day clock value in real-time processing by one or more processors of the computing environment.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:66-8:5 8:6-12 8:13-21 8:22-29 8:43-53 8:62-67 9:13-15 11:23-35 11:61-12:6 14:61-15:4 Figs. 1, 4, 6, 7, 8, 9, 10, 11, 12, 13	

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
The article of manufacture of claim 33, further comprising computer readable program code means for causing a computer to provide as a further part of said sequence value a placeholder value usable in ensuring that said sequence value is an increasing sequence value, even when a physical clock used to provide said timing information of said sequence value wraps back to zero.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 6:31-7:3 8:43-53 8:62-67 9:1-2 12:42-50 12:51-64 14:61-15:4 Figs. 1, 4, 8, 9, 10, 11, 12, 13	
The article of manufacture of claim 33, further comprising computer readable program code means for causing a computer to provide as a further part of said sequence value a processor identifier.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:56-65 8:43-53 8:62-67 9:11-15 12:7-14 12:15-26 14:61-15:4 Figs. 1, 4, 8, 9, 10, 11, 12, 13	

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
The article of manufacture of claim 33, wherein said computer readable program code means for causing a computer to provide comprises computer readable program code means for causing a computer to retrieve, by an instruction, said timing information from a physical clock,	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:4-12 7:13-55 8:43-53 8:62-67 9:1-5 14:61-15:4 Figs. 1, 4, 5, 8, 9, 10, 11, 12, 13	
The article of manufacture of claim 33, ... and wherein said computer readable program code means for causing a computer to include comprises computer readable program code means for causing a computer to retrieve, by said instruction, said selected information from a storage area.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:66-8:5 8:6-12 8:13-21 8:22-29 8:37-42 8:43-53 8:62-67 9:13-15 14:61-15:4 Figs. 1, 4, 6, 7, 8, 9, 10, 11, 12, 13	

Exhibit C

'789 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
The article of manufacture of claim 33, further comprising computer readable program code means for causing a computer to receive said timing information from a physical clock of said computing environment.	**Intrinsic Evidence** `789 Patent: 14:61-15:17 5:7-29; 14:11-24; 14:25-44; 14:35-60 6:16-30 7:4-12 7:13-55 8:43-53 8:62-67 9:1-5 14:61-15:4 Figs. 1, 4, 5, 8, 9, 10, 11, 12, 13	

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U.S. Patent No. 5,987,495

'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
processor	**Intrinsic Evidence** `495 Patent: 6:66-7:41 Fig. 1 **Extrinsic Evidence** **Processor** - (1) In a computer, a functional unit that interprets and executes instructions. A processor consists of at least an instruction control unit and an arithmetic and logic unit. *IBM Dictionary of Computing*, 10th Ed., p. 533 © 1994.	IBM Dictionary of Computing, "processor." Oxford English Dictionary, "processor," "central." October 1, 1989 license agreement between IBM and Intel The document bearing Bates number IBMPSI10152467 http://www.research.ibm.com/journal/rd/511/berger.html http://www-03.ibm.com/systems/browse/inpro/ http://www-03.ibm.com/systems/browse/power/index.html http://www-03.ibm.com/systems/browse/amdpro/index.html?cm_re=masthead-_-products-_-sys-amd https://www-304.ibm.com/systems/support/supportsite.

Exhibit C

'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
		wss/docdisplay?lndocid=MIGR-39433&brandind=5000008 http://www-304.ibm.com/jct09002c/isv/tech/faq/individual?oid=2:85007 http://www-03.ibm.com/press/us/en/pressrelease/21580.wss http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ119954 http://www.intel.com/pressroom/kits/itanium2/ Abstract; 2:5-4:20; 5:29-47; 6:1-17; 7:21-56

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'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
instruction	**Intrinsic Evidence** `495 Patent: Abstract 5:4-29 7:21-41 8:59-9:4 9:23-34 10:32-11:20 Figs. 2A, 3A, 6 **Extrinsic Evidence** **Instruction** - in digital computer operations, a set of bits defining an operation. Consists of an operation code specifying the operation to be performed, one or more operands or their address, and one or more modifiers or their addresses (to modify the operand or its address). *The Illustrated Dictionary of Electronics*, 7th Ed., p. 363, © 1997. **Instruction** - (1) A language construct that specifies an operation and identifies its operands, if any. *IBM Dictionary of Computing*, 10th Ed., p. 346 © 1994.	IBM Dictionary of Computing, "computer instruction," "computer instruction set," "instruction," "machine instruction." *Encyclopedia of Computer Science* (3d ed.) at 684. http://www-306.ibm.com/software/globalization/terminology/ij.jsp The document bearing Bates number IBMPSI03906987 The document bearing Bates number IBMPSI10152467 2:5-4:20; 4:56-6:63; 7:22-56; 9:23-11:19.
program status word	**Intrinsic Evidence** `495 Patent: 2:5-10 7:42-44 7:49-52	http://www-306.ibm.com/software/globalization/terminology/op.jsp#p15 IBM Dictionary of Computing, "program

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'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
	9:65-10:7 10:20-25 Enterprise Systems Architecture/390 Principles of Operation (1994), Order No. SA22-7201-02, Chapter 4 **Extrinsic Evidence** **program status word (PSW)** - (A) A computer word that contains information specifying the current status of a computer program. The information may include error indicators, the address of the next instruction to be executed, currently enabled interrupts, and so on. *The IEEE Standard Dictionary of Electrical and Electronics Terms*, 6th Ed., p. 827, IEEE Std 100-1996. **program status word (PSW)** - An area in storage used to indicate the order in which instructions are executed, and to hold and indicate the status of the computer system. Synonymous with processor status word. *IBM Dictionary of Computing*, George McDaniel, Tenth Edition (August 1993), (c) 1994, ISBN 0-07-031489-6, p. 539. T3 Technologies Liberty Series ML 5.1 Operator Station User Guide	status word." z/Architecture Principles of Operation at 2-2 through 2-5. Abstract; Fig. 1; Fig. 5; Fig. 6; Fig. 8; 1:1-11:19.

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'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
register	**Intrinsic Evidence** `495 Patent: 7:42-56 Fig. 1 **Extrinsic Evidence** **register** - A part of internal storage having a specified storage capacity and usually intended for a specific purpose. *IBM Dictionary of Computing*, George McDaniel, Tenth Edition (August 1993), (c) 1994, ISBN 0-07-031489-6, p. 539.	Encyclopedia of Computer Science, "register." Oxford English Dictionary, "register." The Academic Press Dictionary of Science and Technology, "register." American Heritage Dictionary of the English Language, "register" ("A part of the central processing unit used as a storage location."), *at* http://www.bartleby.com/61/55/R0125500.html. Free On-Line Dictionary of Computing, "register", *at* http://foldoc.org/?register. Abstract; 5:18-6:39; 8:31-10:61.
means for decoding an instruction from a program executing in said problem state specifying a storage location containing a saved program status word	**Intrinsic Evidence** `495 Patent: 5:4-11 6:66-7:11 7:21-28 Fig. 1	

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'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
means responsive to said decoding means for restoring from the saved program status word contained at said specified storage location only those fields of the current program status word that are alterable by a program executing in said problem state.	**Intrinsic Evidence** `495 Patent: 5:4-11 7:21-28 8:52-58 9:45-57 9:65-10:31 10:32-11:5 Figs. 1, 4, 5, 6, 8	*Linking Language:* 6:57-58.
means for determining said storage location using the contents of the register specified by said field.	**Intrinsic Evidence** `495 Patent: 5:4-11 7:21-28 8:52-58 8:56-65 9:15-22 Figs. 1, 2A, 6	*Linking Language:* 9:5-9:22.
means for restoring said saved register contents to said register from said save area.	**Intrinsic Evidence** `495 Patent: 5:4-11 7:21-28 9:10-12 9:36-38 9:58-64 10:46-53 Figs. 1, 2B, 6	*Linking Language:* 10:32-11:19.
means for decoding a program instruction specifying a register selected from said set of registers, said register pointing to a save area	**Intrinsic Evidence** `495 Patent: 5:4-11	

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'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
containing a saved program status word and saved register contents	6:66-7:11 7:21-28 Fig. 1	
means response to said decoding means for executing said instruction, said executing means comprising:	**Intrinsic Evidence** `495 Patent: 5:4-11 6:66-7:11 7:21-4 Fig. 1	
means for accessing said save area using the contents of the register specified by said program instruction	**Intrinsic Evidence** `495 Patent: 5:4-11 7:21-28 8:52-58 8:59-9:4 9:5-22 9:23-34 10:42-45 10:46-50 10:54-59 10:62-66 Figs. 1, 2A, 2B, 3A, 6	

Exhibit C

'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
means for restoring said program status word and said register from the saved program status word and saved register contents contained in said save area to resume execution at the instruction address contained in said saved program status word with the program context defined by said saved program status word and saved register contents.	**Intrinsic Evidence** `495 Patent: 5:4-11 7:21-28 8:59-9:4 9:23-34 9:58-64 10:50-53 10:59-61 10:66-11:2 Figs. 1, 2A, 3A, 6, 8	*Linking Language:* 10:32-11:19.
means for adding the specified displacement to the base address contained in said specified register.	**Intrinsic Evidence** `495 Patent: 5:4-11 7:21-28 9:23-35 9:38-44 9:45-57 10:42-45 Figs. 1, 3A, 3B, 6	
means for adding the offset specified by said program instruction to the beginning address of the save area specified by said register.	**Intrinsic Evidence** `495 Patent: 5:4-11 7:21-28 8:59-9:4 9:5-15 9:23-38 10:46-50 10:54-59 10:62-66	

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'495 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
	Figs. 1, 2A, 2B, 3A, 3B, 6	

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U.S. Patent No. 5,414,851

'851 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
input/output control blocks	**Intrinsic Evidence** `851 Patent: Figs: 4, 8, 10-15, 16a-b 3:60-4:30 7:43-8:68 12:22-55 12:66-13:25 14:66-15:25 15:41-62 16:30-20:54 **Extrinsic Evidence** **Control Block** - (1) A storage area used by a computer program to hold control information. *IBM Dictionary of Computing*, 10th Ed., p. 143, © 1994.	Fig. 4, 6, 9, 10, 12, 14, 3:62-4:10, 7:43-8:61, 12:16-20, 14:46-54, 16:33-35, 25:40-58. International Business Machines Corporation, *ES Architecture 390 ESCON I/O Interface* (1990).
accessing a control block in said sharing set of input/output control blocks, accessed in the just previous step, with an image identifier of one of said plurality of programs	**Intrinsic Evidence** `851 Patent: Figs. 8, 11, 13, 17, 18 12:25-30 12:46-49 13:15-20 16:10-30 17:5-10 21:25-55 **Extrinsic Evidence** **Access** (Computer Programming) - to locate a unit of code or data in memory and use it in a process. *Academic Press Dictionary of Science and Technology*, p. 14, © 1992.	27:64-28:4; Fig. 1; Fig. 17, Fig. 18,

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U.S. Patent No. 5,953,520

'520 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
processor	**Intrinsic Evidence** `520 Patent: Figs. 1, 2, 3 1:60-2:20 2:66-3:29 4:19-7:11 3:15-20 4:19-23 16:1-9 **Extrinsic Evidence** **Processor** – In a computer, a functional unit that interprets and executes instructions. A processor consists of at least an instruction control unit and an arithmetic and logic unit. *IBM Dictionary of Computing,* 10th Ed., p. 533, © 1994.	IBM Dictionary of Computing, "processor." Oxford English Dictionary, "processor," "central." October 1, 1989 license agreement between IBM and Intel The document bearing Bates number IBMPSI10152467 http://www.research.ibm.com/journal/rd/511/berger.html http://www-03.ibm.com/systems/browse/inpro/ http://www-03.ibm.com/systems/browse/power/index.html http://www-03.ibm.com/systems/browse/amdpro/index.html?cm_re=masthead-_-products-_-sys-amd https://www-304.ibm.com/systems/support/supportsite.wss/docdisplay?lndocid=MIGR-39433&brandind=5000008 http://www-304.ibm.com/jct09002c/isv/tech/faq/individual?oid=2:85007 http://www-03.ibm.com/press/us/en/pressrelease/21580.wss http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ119954 http://www.intel.com/pressroom/kits/itanium2/

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'520 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
		Abstract; Figs. 1-3; 1:45-3:33; 4:19-7:11.
instruction set	**Intrinsic Evidence** `520 Patent: Figs. 1, 2, and 3 1:46-3:29 4:19-42 10:45-47 16:1-9  `235 patent (incorporated by reference) 1:14-16; 2:40-46; claim 9 `575 Patent (incorporated by reference) 1:47-50; 1:61-65; 3:46-65 **Extrinsic Evidence** The complete set of instructions recognized by a given computer or provided by a given programming language. *Note*: In computer hardware, this term is considered to be synonymous with a computer's architecture. *The IEEE Standard Dictionary of Electrical and Electronic Terms*, 6th Ed., p. 529, IEEE Std 100-1996. *IBM Microelectronics, PowerPC User Instruction Set Architecture* U.S. Patent No. 7,092,869	IBM Dictionary of Computing, "computer instruction set." *IBM Microelectronics, PowerPC 604 RISC Microprocessor User's Manual, Order No. MPR604UMU-01.* *Intel Corporation, Microprocessors, Publ. No. 230843 (1993).* *MC68030—Enhanced 32-bit Microprocessor User's Manual (1990).* The document bearing Bates number IBMPSI10152467 Abstract; 1:35-53; 4:19-49.

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'520 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
semantic routine	**Intrinsic Evidence** `520 Patent: Figs. 2, 3, 4, 7, and 8 2:6-15 2:65-3:29 4:43-5:6 7:12-46 8:25-55 11:3-64 16:1-9  `235 Patent (incorporated by reference) 1:35-39; 2:49-52 **Extrinsic Evidence** **Routine** - A generic term for any section of code that can be invoked (executed) within a program. *Microsoft Press Computer Dictionary*, 2nd Ed., p. 344 © 1994. **Routine** - A standard practice: regular course of procedure. Webster's Third New International Dictionary, p. 1981 © 1993	Abstract; 2:12-12:19. Compact Oxford English Dictionary, "Routine" ("noun 1 a sequence of actions regularly followed; a fixed unvarying programme."), *at* http://www.askoxford.com/concise_oed/routine. Merriam-Webster's Online Dictionary "Routine" ("4: a sequence of computer instructions for performing a particular task"), *at* http://www.merriam-webster.com/cgi-bin/dictionary?book=Dictionary&va=routine. The document bearing Bates number IBMPSI10152467

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'520 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
means, responsive to receipt of said guest memory access instruction for emulation, for translating said guest logical address into a guest real address and for thereafter translating said guest real address into a native physical address	**Intrinsic Evidence** `520 Patent: Figs. 1, 2, 3, 5, 6, 7, 8 3:21-29 9:22-11:2 12:20-13:51 13:52-14:45 14:46-15:7 15:56-65	*Linking Language:* 3:55-63.
means for executing a semantic routine that emulates said guest memory access instruction utilizing said native physical address.	**Intrinsic Evidence** `520 Patent: Figs. 1, 2, 3, 5, 6, 7, 8 1:64-2:2 2:66-3:2 3:15-29 4:19-5:6 6:25-7:3 8:25-55 11:4-64 13:60-14:20 15:56-67 16:1-9	*Linking Language:* 3:55-63.

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U.S. Patent No. 6,009,261

'261 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
patching instruction	**Intrinsic Evidence** `261 Patent: Figs. 3-13, 19, 20 Abstract 5:46-56 8:39-9:5 10:20-31 10:56-63 11:15-55 12:62-13:5 13:45-63 13:66-15:23 16:20-21 16:53-17:9 17:22-48 18:65-19:4	4:27-29; 13:55-59; 3:60-4:45.

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'261 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
incompatible instruction	**Intrinsic Evidence** `261 Patent: Abstract 3:61-5:28 5:46-7:42 8:37-11:40 12:46-15:44 15:45-19:20 Figs. 1-20 **Extrinsic Evidence** **Instruction** - in digital computer operations, a set of bits defining an operation. Consists of an operation code specifying the operation to be performed, one or more operands or their address, and one or more modifiers or their addresses (to modify the operand or its address). *The Illustrated Dictionary of Electronics*, 7th Ed., p. 363, © 1997. **Instruction** - (1) A language construct that specifies an operation and identifies its operands, if any. *IBM Dictionary of Computing*, 10th Ed., p. 346 © 1994. U.S. Patent No. 7,092,869	IBM Dictionary of Computing, "computer instruction," "computer instruction set," "instruction," "machine instruction." *Encyclopedia of Computer Science* (3d ed.) at 684. http://www-306.ibm.com/software/globalization/terminology/ij.jsp The document bearing Bates number IBMPSI03906987 The document bearing Bates number IBMPSI10152467 Abstract; Fig. 3; Fig. 9; 3:60-7:51; 8:37-19:14

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'261 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
target instruction	**Intrinsic Evidence** `261 Patent: Abstract 3:61-5:28 5:46-7:42 8:37-11:40 12:46-15:44 15:45-19:20 Figs. 1, 3-20 **Extrinsic Evidence** **Instruction** - in digital computer operations, a set of bits defining an operation. Consists of an operation code specifying the operation to be performed, one or more operands or their address, and one or more modifiers or their addresses (to modify the operand or its address). *The Illustrated Dictionary of Electronics*, 7th Ed., p. 363, © 1997. **Instruction** - (1) A language construct that specifies an operation and identifies its operands, if any. *IBM Dictionary of Computing*, 10th Ed., p. 346 © 1994. U.S. Patent No. 7,092,869	IBM Dictionary of Computing, "computer instruction," "computer instruction set," "instruction," "machine instruction." *Encyclopedia of Computer Science* (3d ed.) at 684. http://www-306.ibm.com/software/globalization/terminology/ij.jsp The document bearing Bates number IBMPSI03906987 The document bearing Bates number IBMPSI10152467 Abstract; Fig. 3; Fig. 9; 3:60-7:51; 8:37-19:14

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'261 Claim Term	IBM's Intrinsic and Extrinsic Support	PSI's Intrinsic and Extrinsic Support
processor	**Intrinsic Evidence** `261 Patent: Figs. 1, 3, 10-15 Abstract 3:62-65 4:7-12 4:30-35 5:46-48 8:37-49 8:56-65 11:16-17 13:55-65 14:4-6 18:65-19:4 **Extrinsic Evidence** **Processor** – In a computer, a functional unit that interprets and executes instructions. A processor consists of at least an instruction control unit and an arithmetic and logic unit. *IBM Dictionary of Computing,* 10th Ed., p. 533, © 1994.	IBM Dictionary of Computing, "processor." Oxford English Dictionary, "processor," "central." October 1, 1989 license agreement between IBM and Intel The document bearing Bates number IBMPSI10152467 http://www.research.ibm.com/journal/rd/511/berger.html http://www-03.ibm.com/systems/browse/inpro/ http://www-03.ibm.com/systems/browse/power/index.html http://www-03.ibm.com/systems/browse/amdpro/index.html?cm_re=masthead-_-products-_-sys-amd https://www-304.ibm.com/systems/support/supportsite.wss/docdisplay?lndocid=MIGR-39433&brandind=5000008 http://www-304.ibm.com/jct09002c/isv/tech/faq/individual?oid=2:85007 http://www-03.ibm.com/press/us/en/pressrelease/21580.wss http://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ119954 http://www.intel.com/pressroom/kits/itanium2/ Abstract; Fig. 1; Fig. 10; 1:30-19:20.

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'261 Claim Term	**IBM's Intrinsic and Extrinsic Support**	**PSI's Intrinsic and Extrinsic Support**
target routine	**Intrinsic Evidence** `261 Patent: Figs. 2-5, 9, 19, 20 Abstract 5:8-17 5:47-56 6:24-65 7:28-41 8:37-9:5 9:35-61 10:6-19 11:16-23 13:11-18 13:45-65 14:44-46 15:13-23 16:5-19 18:15-59 **Extrinsic Evidence** **Routine** - A generic term for any section of code that can be invoked (executed) within a program. *Microsoft Press Computer Dictionary*, 2nd Ed., p. 344 © 1994. **Routine** - A standard practice: regular course of procedure. Webster's Third New International Dictionary, p. 1981 © 1993	Abstract, 4:23-45; 5:8-17, 5:18-22, 6:38-40; 8:48; 8:66-9:5, 9:35-48, 10:13-16, 11:16-23, 11:33-38, 19:41-64. Compact Oxford English Dictionary, "Routine" ("noun 1 a sequence of actions regularly followed; a fixed unvarying programme."), *at* http://www.askoxford.com/concise_oed/routine. Merriam-Webster's Online Dictionary "Routine" ("4: a sequence of computer instructions for performing a particular task"), *at* http://www.merriam-webster.com/cgi-bin/dictionary?book=Dictionary&va=routine. The document bearing Bates number IBMPSI10152467